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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/666,688	09/18/2003	Thomas S. Wong	MIC-M084	1405
32566	7590	12/07/2005	EXAMINER	
PATENT LAW GROUP LLP 2635 NORTH FIRST STREET SUITE 223 SAN JOSE, CA 95134			WELLS, KENNETH B	
			ART UNIT	PAPER NUMBER
			2816	

DATE MAILED: 12/07/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

AK

**Office Action Summary**

Application No.

10/666,688

Applicant(s)

WONG ET AL.

Examiner

Kenneth B. Wells

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 01 December 2005.
- 2a) ☐ This action is **FINAL**.                      2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-3,5,7-11,13 and 15 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 1-3,5,7-11 and 13 is/are allowed.
- 6) ☒ Claim(s) 15 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All    b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)  | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                                   | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)             |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____  |

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1. The response filed on 12/1/05 has been received and entered in the case. In view of the arguments therein, the previous rejection based on Murden is now withdrawn. However, in view of newly discovered prior art, new rejections are now set forth. Any inconvenience caused by the delay in citing this new prior art is regretted.

2. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

3. Claim 15 is rejected under 35 U.S.C. 102(b) as being anticipated by Kobayashi or Holloway et al.

Note Fig. 4 of Kobayashi, where the emitter follower is the combination of BJT Q4, isolation resistor R1 and current source R2. The limitation that the isolation resistor has a value which reduces in-rush current is deemed to be inherent in Kobayashi's Fig. 4 circuitry, because it appears that any resistor value will reduce the claimed in-rush current.

Note also Fig. 1 of Holloway et al, where the emitter follower is the combination of BJT Q5, isolation resistor R3 and current source R4. The limitation that the isolation resistor has a value which reduces in-rush current is deemed to be

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inherent in Holloway's Fig. 1 circuitry, because it appears that any resistor value will reduce the claimed in-rush current.

4. Claim 15 is rejected under 35 U.S.C. 102(e) as being anticipated by Visocchi.

Note Fig. 2, where the emitter follower is the combination of BJT Q3, isolation resistor R3 and current source 208. The limitation that the isolation resistor has a value which reduces in-rush current is deemed to be inherent in Visocchi's Fig. 2 circuitry, because it appears that any resistor value will reduce the claimed in-rush current.

5. Claim 15 is rejected under 35 U.S.C. 102(b) as being anticipated by Smetana.

Note Fig. 4B, where the emitter follower is the combination of BJT Q16, isolation resistor R18 and the current source formed by the combination of Q17 and R19. The limitation that the isolation resistor has a value which reduces in-rush current is deemed to be inherent in Smetana's Fig. 4B circuitry, because it appears that any resistor value will reduce the claimed in-rush current.

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6. Claim 15 is rejected under 35 U.S.C. 102(b) as being anticipated by Nagase et al.

Note Fig. 10, where the emitter follower is the combination of BJT Q2, isolation resistor R6 and current source R7. The limitation that the isolation resistor has a value which reduces in-rush current is deemed to be inherent in Nagase et al's Fig. 10 circuitry, because it appears that any resistor value will reduce the claimed in-rush current.

7. Claim 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over any one of Kobayashi, Visocchi, Smetana and Nagase et al.

To the extent that the above-noted references do not disclose the value of the isolation resistor that will reduce in-rush current, those having ordinary skill in the art will easily recognize that R1 can be set to any value and thus the limitation "to reduce in-rush current..." does not define patentably over the above-noted references.

8. Claim 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over Fuji.

Note Fig, 7, where the emitter follower is the combination of BJT T22, isolation resistor R11 and current source T11. The limitation that the isolation resistor has a value which reduces

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in-rush current is deemed to be inherent Fuji's Fig. 10 circuitry, because it appears that any resistor value will reduce the claimed in-rush current. The only difference between claim 15 and Fuji is that the isolation resistor R11 in Fuji is not between the emitter of T22 and the current source, but rather the current source is between the emitter of T22 and the resistor. However, because it is old and well-known in the art that when forming, in an IC, a series combination of a resistor and a current source, the order of the two elements is irrelevant (the function will be identical). Thus, claim 15 does not define patentably over Fuji under 35 U.S.C. 103.

9. Claims 1-3, 5, 7-11 and 13 are allowed.

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Note USP 6,683,896; 6,618,406; and 6,437,630 which teach further emitter follower circuits with the resistor and current source combinations reversed (similar to Fuji's Fig. 7).

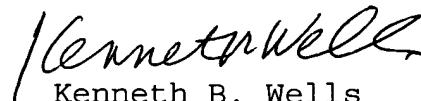
11. In view of the above-noted new grounds of rejection, this office action is non-final.

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12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kenneth B. Wells whose telephone number is (571)272-1757. The examiner can normally be reached on Monday through Friday from 8:30am to 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy P. Callahan, can be reached at (571)272-1740. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information Business Center (EBC) at 866-217-9197 (toll-free).



Kenneth B. Wells  
Primary Examiner  
Art Unit 2816

December 6, 2005